“Known Good Die: More of The Story”

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Agenda

• KGD Status

• **How We Got Here:**
  – Case #1 Hybrids
  – Case #2 MCM-D
  – Case #3 Memory Devices

• **What Does This History Suggest？**
  – Reworkable Structures
  – “Always Good” Die
  – Self-Repair

• **Conclusion**
20 Years “Searching/Desiring” KDG

• No argument that KGD are/would be beneficial
• Memory Die Are the Primary Available KGD.
• **Maybe We Should Consider Some Alternatives**
• What Might They Be?

Let’s Consider This a Workshop Rather Than a “Talk”.

How We Got to KGD

• **Classic hybrids**
• Thin film Multichip Modules; MCM: D
• Memory Devices
• **SiP on FR-4, BT, etc.**
Case #1. Classic Hybrid Examples
Example #1

0.100” pitch through-hole leads
6 die, several SMT parts
Black items on substrate are resistors +/- 1%
1 mil Gold wire, thermosonic ball bonding
Example #2

0.050” pitch through-hole leads, DIP Configuration
6 die, 7 SMT parts
Blue is a glaze overcoat
1 mil Aluminum wire, ultrasonic wedge bonding
Example #3

0.050” pitch, SMT wrap around leads
20 die, 12 SMT parts, ~24 chip transistors, ~20 chip caps, 6 embedded resistors
1 mil Aluminum wire, ultrasonic wedge bonding
Example #4

0.100” pitch through-hole leads, DIP configuration
12 die, 8 SMT parts, ~10 embedded resistors
1 mil Aluminum wire, ultrasonic wedge bonding
Example #5

0.100” pitch through-hole leads, SIP configuration
2 die, 7 SMT parts, ~12 chip components, ~20 embedded resistors
1 mil Aluminum wire, ultrasonic wedge bonding
Chip & Wire Hybrids

- **Build on ceramic platform with Thick Film Inks**
  - Ceramic and Glass Dielectrics Fired at >650C
  - Metal layers ~20 microns thick
  - >100 micron lines and spaces
  - Up to 30 layers
  - Through hole connections available
  - Embedded resistors with +/- 1% tolerance

- **Assembly**
  - Epoxy die attach
  - Aluminum ultrasonic wedge & Gold thermosonic wire bonding

- **Reworkable**

- **Defective Die found in test and REPLACED**

- **So Built WITHOUT KGD !!**
Case #2. Thin Film Multi Chip Modules: MCM-D
Mil Class MCM

- Module for standard SEM card
- Hermetic ceramic solder sealed package
- 0.050” pitch leads
- Epoxy Die attach
- Sn63 SMT
Multi-Die Package

224 IO on 0.050” pitch
Co-fired ceramic package
Epoxy die attach

Au thermosonic wire bonding
Sn63 SMT
Solder seal lid
Memory Module

12 memory die & 2 caps
Die mounted “flip chip” using BIP, Bonded interconnect pin
MCM-D Cross Section

- 5 micron sputtered metal layers; Al or Cu
- 5 layers max
- Polyimide Dielectric: $e = 3.4$, 1% H2O uptake, 10 micron layers
- 25 micron lines; 50 micron space
- $\text{Al}_2\text{O}_3$ or Silicon substrate
- Solderable, die attach and wire bondable finishes
Case #2. Multi Chip Modules

- Made with Polyimide and BCB dielectrics
  - Tg of 300C
  - Thin film metal
  - Thin Film structures are not as robust as Thick Film
  - Rework difficult to impossible
- Substrates are not robust enough for Rework
- Hence the Need for KGD!
Case #3. Memory Devices

• Redundancy built into die !!
• Some defects are tolerable
• Designed-in Functionality automatically corrects the results
  – Utilize error correction codes
  – Adding 2 extra bits to a “word” enable correction of 1 incorrect bit
What Alternatives to KGD Do These 3 Cases Suggest?

1. **Reworkable Assemblies that Allow Defective Die to be Found and Replaced Easily.**

2. Die that are “Always good”.

3. **Systems That Tolerate Defects and Failures.**
#1 Reworkable Assemblies

- **Structures, Processes & Parts that Can be Reworked Easily**

- Need multi layer structures with lines and spaces of <10 microns.
  - Substrates Built with Semiconductor Global Interconnect-Like Technology? Cost? Functionality inadequate?
  - Eliminate the Organic Dielectric and Improve Robustness?

- **What about a Fine Line Thick Film Technology?**
  - Can we Overcome the (100 micron) Line & Space Screen Printing Limit?

- **In All Cases, Cost Effective, Methods to Find and Replace Defective Parts Are Needed.**
#2 “Always Good” Die Issues

- **An “Always Good” Design Philosophy is Not Known**
  - Design Methods Assume Everything Works as Desired
  - Redundancy is Eliminated to “Reduce Cost”.
    - Is That really true?
  - CAD Tools Are Not Available

- **Net Cost Impact Is Unclear:**
  - **Pros**
    - Eliminate Testing
    - Eliminates Post Packaging Final Scrap Cost
  - **Cons**
    - Requires more chip area
      - How much is unclear
      - Varies by function

- **Does Current Philosophy “Kick the Can” down the Chain?**

- **A More Specific Question/View Might Be:**

  “What Die Functionalities Can Cost Effectively Incorporate “Always Good” Redundancy?”
#3 Design Chip Sets & Package Combinations that Can Tolerate Faults

- **Chip Sets That are able to detect and “work around” defects**
  - Design in redundancy
  - Design for self repair

- **Again, Need a Methodology and Design Tools**

- **Similar to Always Good Die but at the System Level**
Conclusion

Known Good Die Would Be Wonderful,

BUT:

We Have Only a Few After 20 Years.

Maybe We Should Consider Alternatives:

1. Develop Materials and Processes to Enable Low Cost Replacement of Defective Die

2. Change The Up Front Chip Design & Fab Methodology To Fabricate Die That are “Always Good”.

3. Design Chips And Systems That Have Enough Redundancy to Self Repair